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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04B 7/185, G01S 5/02 — A1

(11) International Publication Number: WO 95/19666

(43) International Publication Date: 20 July 1995 (20.07.95)

(21) International Application Number: PCT/US95/00325

(22) International Filing Date: 12 January 1995 (12.01.95)

(30) Priority Data:
08/186,393 14 January 1994 (14.01.94) US

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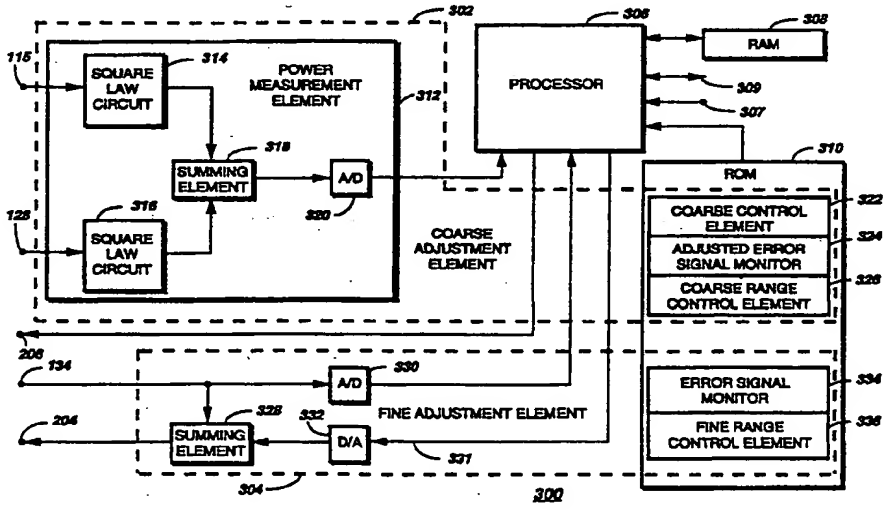
(81) Designated States: CA, CN, KR, MX, RU, UA, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: SATELLITE RECEIVER SYSTEM HAVING DOPPLER FREQUENCY SHIFT TRACKING



(57) Abstract

A satellite receiver system (400) provides acquisition and frequency tracking of a Doppler-shifted radio signal received from an orbiting satellite. The satellite receiver system (400) includes a Costas phase-lock loop (100) that receives the radio signal and provides an error signal at an error signal output (134) for controlling a conversion frequency generated by a voltage controlled oscillator (200). The voltage controlled oscillator (200) is coupled to the Costas phase-lock loop (100) and generates the conversion frequency for down-converting the radio signal in the Costas phase-lock loop (100). The satellite receiver system (400) further includes a Doppler frequency acquisition and tracking element (300) coupled to the voltage controlled oscillator (200). The Doppler frequency acquisition and tracking element (300) adjusts the conversion frequency to compensate for a Doppler frequency shift occuring in the radio signal due to orbital motion of the orbiting satellite.

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SATELLITE RECEIVER SYSTEM HAVING DOPPLER FREQUENCY SHIFT TRACKING

Field of the Invention

This invention relates in general to radio communication receivers, and more specifically to a radio communication receiver system that provides frequency tracking of a Doppler shifted radio signal.

Background of the Invention

Communication systems utilizing direct transmission of signals from orbiting satellites to Earth-based receivers are well known. Such systems have been described in U.S. Patent No. 5,121,503 to Davis, entitled "Satellite Signaling System Having a Signal Beam with a Variable Beam Area," and in U.S. Patent No. 5,239,670 to Schwendeman et al., entitled "Satellite Based Global Paging System." Said U.S. Patents are hereby incorporated herein by reference.

A radio signal transmitted from a non-geostationary satellite, e.g., a Low Earth Orbit satellite, can present reception difficulties due to large Doppler frequency shifts caused by orbital motion of the satellite. Because of the high cost of transmitter power in satellite communication systems, earth based receivers used in such systems require high sensitivity to achieve adequate system gain. High sensitivity can be achieved by utilizing a narrow bandwidth, phase coherent receiver, such as a binary phase shift keyed (BPSK) receiver, and further by utilizing differential encoding for the transmitted data.

Unfortunately, the Doppler frequency shift in such a system can be significantly larger than the receiver bandwidth required for high sensitivity. This condition makes it impossible for the receiver to acquire the radio signal except during a brief period in which the satellite is most directly overhead, and thus is producing a limited velocity component with respect to the receiver. Without the Doppler frequency shift, it would be possible for the receiver to receive the satellite transmissions for a much greater period during which the satellite antenna is "in view" of the receiver antenna.

Thus, what is needed is a satellite receiver system that provides acquisition and frequency tracking of a Doppler shifted radio signal to allow narrow-band reception of the radio signal from an orbiting satellite for substantially the entire period during which the satellite is in view of the satellite receiver system.

Summary of the Invention

A satellite receiver system provides acquisition and frequency tracking of a Doppler-shifted radio signal received from an orbiting satellite. The satellite receiver system comprises a Costas phase-lock loop that receives the radio signal and provides an error signal at an error signal output for controlling a conversion frequency generated by a voltage controlled oscillator. The voltage controlled oscillator is coupled to the Costas phase-lock loop and generates the conversion frequency for down-converting the radio signal in the Costas phase-lock loop. The satellite receiver system further comprises a Doppler frequency acquisition and tracking element coupled to the voltage controlled oscillator. The Doppler frequency acquisition and tracking element adjusts the conversion frequency to compensate for a Doppler frequency shift occurring in the radio signal due to orbital motion of the orbiting satellite.

Brief Description of the Drawings

FIG. 1 is an electrical block diagram of a conventional Costas phase-lock loop.

FIG. 2 is an electrical block diagram of a conventional two-stage synthesized voltage controlled oscillator.

FIG. 3 is an electrical block diagram of a Doppler frequency acquisition and tracking element in accordance with the preferred embodiment of the present invention.

FIG. 4 is an electrical block diagram of a satellite receiver system in accordance with the preferred embodiment of the present invention.

FIG. 5 is a flow chart depicting operation of a processor and a coarse adjustment element in accordance with the preferred embodiment of the present invention.

FIG. 6 is a flow chart depicting operation of the processor and a fine adjustment element in accordance with the preferred embodiment of the present invention.

FIG. 7 is an electrical block diagram of an error signal monitor element in accordance with an alternative embodiment of the present invention.

Description of the Preferred Embodiment

Referring to FIG. 1, an electrical block diagram of a conventional Costas phase-lock loop 100 comprises a received signal input 102 coupled to first and second mixers 108, 120 for receiving a radio signal. The first mixer 108 receives a conversion frequency directly from a conversion frequency input 103. The second mixer 120 receives the same conversion frequency, phase shifted by ninety degrees in a phase shift element 118. The first and second mixers 108, 120 are coupled through first and second amplifiers 110, 122 and first and second baseband data filters 112, 124 to produce in-phase (I) and quadrature (Q) signals at first and second nodes 114, 126, respectively. The first and second nodes 114, 126 are coupled to a third mixer 130, which is coupled through an automatic frequency control (AFC) filter 132 to produce an error signal at an error signal output 134 for controlling the conversion frequency generated by a voltage controlled oscillator 200 (FIG. 2), as described herein below. The first and second nodes 114, 126 also are coupled to first and second power measurement outputs 115, 128, and thence to a power measurement element 312 (FIG. 3) for measuring received power of the radio signal. The first node 114 is further coupled to a limiter 116 for producing a demodulated data bit stream at a data output 106. The first mixer 108, the first amplifier 110, the first baseband data filter 112 and the limiter 116 form a demodulation element 104 for demodulating the radio signal to derive the demodulated data bit stream. The modulation is preferably differentially encoded binary phase-shift keyed (DE-BPSK) modulation. It will be appreciated that double sideband amplitude modulation and non-differentially encoded BPSK modulation can be demodulated as well by the Costas phase-lock loop 100.

Referring to FIG. 2, an electrical block diagram of a conventional two-stage synthesized voltage controlled oscillator (VCO) 200 comprises a fine frequency control input 204 and a stepped frequency programming input 206. The fine frequency control input 204 is coupled to a first varactor

diode 212 for "warping" a frequency generated by a first VCO 210 controlled by a reference crystal 214. The first VCO 210 is utilized in a conventional manner to generate a frequency reference for a programmable frequency synthesizer 203. The stepped frequency programming input 206 is coupled to the programmable frequency synthesizer 203 to allow selection of one of a plurality of output frequencies selectable in steps. An error output 216 of the programmable frequency synthesizer 203 is coupled to a second varactor diode 218 for warping a frequency generated by a second VCO 220. The frequency generated by the second VCO 220 is available at a VCO output node 208, which is coupled to a count-down input 222 of the programmable frequency synthesizer 203 for feedback and count-down of the frequency generated by the second VCO 220 in a conventional manner. The VCO output node 208 is also coupled to the conversion frequency input 103 of the Costas phase-lock loop 100 (FIG. 1) for supplying the conversion frequency utilized for down converting the received radio signal to baseband.

Referring to FIG. 3, an electrical block diagram of a Doppler frequency acquisition and tracking element 300 in accordance with the preferred embodiment of the present invention is depicted. The Doppler frequency acquisition and tracking element 300 comprises a coarse adjustment element 302 for adjusting the conversion frequency generated by the VCO 200 in steps, and a fine adjustment element 304 for providing fine adjustment of the conversion frequency. The Doppler frequency acquisition and tracking element 300 further comprises a processor 306 coupled to the coarse and fine adjustment elements 302, 304 and coupled through the fine adjustment element 304 to the fine frequency control input 204 of the VCO 200. The processor 306 is also coupled to the stepped frequency programming input 206 of the VCO 200, and controls the conversion frequency generated therefrom in response to signals from the coarse and fine adjustment elements 302, 304. The processor 306 is preferably a digital signal processor (DSP) similar to the DSP56000 digital signal processor manufactured by Motorola, Inc. of Schaumburg, Illinois. It will be appreciated that other similar devices can be utilized for the processor 306 as well.

The processor 306 is also coupled to a conventional random access memory (RAM) 308 for temporary storage of operational values and to a conventional read-only memory (ROM) 310, which contains firmware

elements for controlling the Doppler frequency acquisition and tracking element 300 in accordance with the preferred embodiment of the present invention. The processor 306 is further coupled to a bus 309 and a serial data input 307 for communicating with additional elements of a satellite receiver system, as will be described herein below in reference to FIG. 4.

Firmware elements forming a portion of the fine adjustment element 304 comprise an error signal monitor 334 for monitoring an error signal present at the error signal output 134 of the Costas phase-lock loop 100 to determine whether the error signal is within a first predetermined operating range demarked by low and high limits. The firmware elements of the fine adjustment element 304 further comprise a fine range control element 336 wherein, after a radio signal has been acquired, the fine range control element 336 adjusts a fine adjustment signal supplied by the fine adjustment element 304 to generate an adjusted error signal at the fine frequency control input 204 of the VCO 200. The fine adjustment signal is decremented by a fine adjustment value equal to the first predetermined operating range in response to the error signal being below the low limit, and is incremented by the same fine adjustment value in response to the error signal being above the high limit. In this manner the fine adjustment element 304 acts to maintain the error signal within the first predetermined operating range.

Firmware elements forming a portion of the coarse adjustment element 302 comprise a coarse control element 322 for selecting a suitable one of a plurality of frequencies to provide a coarse adjustment of the conversion frequency to compensate for Doppler frequency shift. The firmware elements of the coarse adjustment element 302 further comprise an adjusted error signal monitor 324 for monitoring the adjusted error signal at the fine frequency control input 204 to determine whether the adjusted error signal is within a second predetermined operating range demarked by first and second limits, wherein the conversion frequency corresponding to the first limit is a lower frequency than that corresponding to the second limit. The firmware elements of the coarse adjustment element 302 also include a coarse range control element 326 for controlling the VCO 200 to generate a next lower one of the plurality of frequencies and simultaneously controlling the fine adjustment element 304 to set the adjusted error signal to a value substantially equal to the second limit, in response to the adjusted error signal being outside of the

second predetermined operating range in a direction beyond the first limit.

The fine adjustment element 304 further comprises a first conventional analog-to-digital (A/D) converter 330 for converting the error signal present at the error signal output 134 into a digital value readable by the processor 306. The fine adjustment element 302 also includes a conventional digital-to-analog (D/A) converter 332 for converting a digital representation of the fine adjustment signal on a control path 331 from the processor 306 into an analog signal, which is added with the error signal in a first conventional analog summing element 328 to generate the adjusted error signal at the fine frequency control input 204 of the VCO 200.

The coarse adjustment element 302 further comprises a power measurement element 312, including two conventional square law circuits 314, 316, coupled respectively to the first and second power measurement outputs 115, 128 of the Costas phase-lock loop 100. The output signals from the square law circuits 314, 316 are summed in a second conventional analog summing element 318 to produce a power level signal, which is converted into a digital signal in a second conventional A/D converter 320 for processing by the processor 306. The power level signal is proportional to the received power, i.e., the sum of the squares of the signals I and Q present at the first and second power measurement outputs 115, 128, respectively.

Preferably, the D/A converter 332 and the A/D converters 320, 330 are similar to the D/A and A/D circuits found in the DSP56166 digital signal processor chip manufactured by Motorola, Inc. of Schaumburg, Illinois. The analog summing elements 318, 328 preferably are conventional operational amplifiers available off-the-shelf. Preferably, the square law circuits 314, 316 are similar to the MC1494L/1594L linear four quadrant multiplier manufactured by Motorola, Inc. of Schaumburg, Illinois. It will be appreciated that other similar devices can be used as well for the A/D converters 320, 330, the D/A converter 332, the analog summing elements 318, 328, and the square law circuits 314, 316.

Referring to FIG. 4, an electrical block diagram of a satellite receiver system 400 in accordance with the preferred embodiment of the present invention comprises an antenna 402 coupled through a conventional matching element 404 to a conventional low-noise amplifier (LNA) 406

for receiving and amplifying a radio signal. The LNA 406 is coupled to the received signal input 102 of the Costas phase-lock loop 100 for down-converting and demodulating the radio signal to derive the demodulated data bit stream at the data output 106. The data output 106 is coupled to a conventional bit synchronizer 408 for delivering the demodulated data bit stream to the serial data input 307 of the Doppler frequency acquisition and tracking element 300.

Preferably, the matching element 404, the LNA 406, and the bit synchronizer 408 are similar to those utilized in the model A03KLB5962CA ADVISOR® pager, manufactured by Motorola, Inc. of Schaumburg, Illinois. It will be appreciated that other similar devices can be used as well for the matching element 404, the LNA 406, and the bit synchronizer 408.

The first and second power measurement outputs 115, 128 of the Costas phase-lock loop 100 are also coupled to the Doppler frequency acquisition and tracking element 300 for providing the I and Q signals thereto for power measurement in the power measurement element 312. In addition, the error signal output 134 of the Costas phase-lock loop 100 is coupled to the Doppler frequency acquisition and tracking element 300 for adjustment thereof to correct for Doppler frequency shift in accordance with the preferred embodiment of the present invention. The fine frequency control input 204 and the stepped frequency programming input 206 of the VCO 200 are coupled to the Doppler frequency acquisition and tracking element 300 for controlling the conversion frequency generated from the VCO 200. The VCO 200 is also coupled to the conversion frequency input 103 of the Costas phase-lock loop 100 for supplying the conversion frequency thereto.

The satellite receiver system 400 further comprises a microcomputer 410 coupled to the Doppler frequency acquisition and tracking element 300 by the bus 309. The microcomputer 410 provides control of the satellite receiver system 400 and is preferably similar to the MC68HC05, C08, or C11 series microcomputers, or a DSP56000 series digital signal processor, all manufactured by Motorola, Inc. of Schaumburg, IL. It will be appreciated that other similar devices may be utilized for the microcomputer 410 as well. The microcomputer 410 is also coupled to a display 412, such as a conventional liquid crystal display, for displaying received information. In addition, the microcomputer 410 is coupled to user controls 414, such as well-known buttons and switches for allowing a user to control operation

of the satellite receiver system 400. An alert generator 416, such as a conventional piezoelectric sounder, is also coupled to the microcomputer 410 for alerting the user whenever information intended for the satellite receiver system 400 is received.

The utilization of the Doppler frequency acquisition and tracking element 300 in accordance with the preferred embodiment of the present invention advantageously allows the satellite receiver system 400 to acquire, track, and receive Doppler shifted satellite transmissions for substantially the entire period during which the satellite is in view of the satellite receiver system 400. This is possible even though the satellite receiver system 400 preferably has a narrow receiver bandwidth (required for high sensitivity) substantially smaller than the Doppler frequency shift encountered over the entire period during which the satellite is in view of the satellite receiver system 400. The method by which the satellite receiver system 400 operates to provide Doppler frequency acquisition and tracking will be described further below.

Referring to FIG. 5, a flow chart depicting operation of the processor 306 and the coarse adjustment element 302 in accordance with the preferred embodiment of the present invention begins with start-up 502 of the satellite receiver system 400. Following start-up, the processor 306 accesses the coarse control element 322 and controls the fine adjustment element 304 to set 504 the fine adjustment signal to the middle of its operating range. Then the processor 306 controls 506 the VCO 200 through the stepped frequency programming input 206 to generate a predetermined initial conversion frequency.

The predetermined initial conversion frequency is selected to be a "statistically predominant" Doppler shifted frequency at the time of initial acquisition of a transmission from an approaching satellite. By "statistically predominant" is meant a Doppler shifted frequency that is statistically most likely from an approaching satellite. A satellite that is in view is most likely to pass at an elevation of approximately 35 degrees above the horizon, not directly overhead. This means that the statistically predominant initial Doppler shift for an approaching satellite is a positive shift of substantially less than the maximum possible Doppler shift, i.e., the Doppler shift produced if the satellite passes directly overhead. For example, in the case of a system operating near 1624 MHz, the maximum Doppler shift is ±36 KHz for a Low Earth Orbit satellite passing directly

overhead, while the statistically predominant initial Doppler shift for an approaching satellite is about +20 KHz. Thus, for the example system a good choice of predetermined initial conversion frequency is 20 KHz above the nominal operating frequency of the system.

In addition to adjusting the conversion frequency to compensate for Doppler shift, it is necessary to adjust the conversion frequency to compensate for frequency inaccuracy inherent in the reference crystal 214. For the example system, a ±10 parts per million reference crystal tolerance would produce about ±16 KHz frequency variation, for a total frequency variation of ±52 KHz. The combination of the reference crystal inaccuracy and the uncertain amount of Doppler frequency shift being encountered usually make it necessary to hunt about the predetermined initial conversion frequency in some manner to search for the best frequency for initially acquiring lock with the radio signal from the satellite, as described below.

In step 508 the processor 306 evaluates the signal from the power measurement element 312 to determine if the received power is above a predetermined threshold, e.g., above a level that will insure a sufficiently low bit error rate. If not, the processor 306 controls 510 the VCO 200 to generate a next predetermined conversion frequency, followed by another until the received power is determined to be above the predetermined threshold. For example, a search sequence of +20, +30, +40, +50, +40, +30, +20, +10, 0, -10, -20, -30, -40, -50, -40, -30, -20, -10, 0, +10, +20 KHz, and so forth, preferably is utilized to locate a conversion frequency that initially acquires lock with the radio signal.

When the radio signal has been acquired 512, the processor 306 accesses the adjusted error signal monitor 324 to check 514 whether the adjusted error signal is beyond a predetermined operating range on the low frequency side. The adjusted error signal is the signal present at the fine frequency control input 204 of the VCO 200, the signal comprising the sum of the error signal from the Costas phase-lock loop 100 and the analog fine adjustment signal generated under control of the processor 306 by the fine adjustment element 304. The operating range of the adjusted error signal is limited by the usable frequency warping range of the first varactor diode 212. The reason for checking only the low frequency side of the operating range is that the Doppler shifted frequency of the satellite always decreases monotonically after initial signal acquisition.

If in step 514 the adjusted error signal is not beyond its operating range on the low frequency side, then the processor 306 checks 518 whether the received power as indicated by the power measurement element 312 is still above the predetermined threshold. If so, the processor loops back to step 514 to continue checking for an out-of-range adjusted error signal. If, on the other hand, in step 518 the received power is not above the predetermined threshold, then the radio signal has been lost 520, and the flow returns to step 504 to search for another radio signal.

If in step 514 the adjusted error signal is determined to be beyond its operating range on the low frequency side, then the processor 306 accesses the coarse range control element 326 to control 516 the VCO 200 to generate a next lower predetermined frequency and to simultaneously control the fine adjustment element 304 to set the adjusted error signal to the opposite operating range limit on the high frequency side. Preferably, the net result of step 516 is to produce substantially no change in the conversion frequency generated by the VCO 200. For example, if the next lower frequency generated by the VCO 200 would have been 10 KHz lower, then setting the adjusted error signal to the opposite operating range limit on the high frequency side should move the conversion frequency substantially 10 KHz higher, for a net zero change in frequency. Following step 516, the flow returns to loop through steps 518 and 514 to continue to maintain the adjusted error signal within its operating range until the radio signal is lost.

It will be appreciated that step 516, if executed during the reception of data, would be likely to cause bit errors in the received data. Thus, the coarse range control element 326 preferably limits the execution of step 516 to those times during which data is not being received. Such operation preferably is facilitated by designing the system such that the satellite transmissions send the data in packets of predetermined periodicity separated by intervals of no data, wherein each packet includes initial synchronization information that allows the satellite receiver system 400 to reacquire phase lock to the radio signal following the execution of step 516.

Referring to FIG. 6, a flow chart depicting operation of the processor 306 and the fine adjustment element 304 in accordance with the preferred embodiment of the present invention begins with acquisition 602 of the radio signal by the satellite receiver system 400, as described herein above.

After signal acquisition, the processor 306 accesses the error signal monitor 334 and monitors 604 the error signal from the Costas phase-lock loop 100. If in step 606 the error signal is below a low limit of its predetermined operating range, the processor 306 accesses 608 the fine range control element 336 and decrements the fine adjustment signal by a value equal to the operating range of the error signal, after which flow returns to step 604. The Costas phase-lock loop 100 will quickly increase the error signal to return the adjusted error signal to its former value for maintaining lock with the radio signal. The net result will be to move the error signal to the opposite (high) limit of its operating range, thereby keeping the error signal within the predetermined operating range.

If in step 606 the error signal is not below a low limit of its predetermined operating range, the processor 306 checks 610 whether the error signal is above a high limit of its predetermined operating range. If so, the processor 306 increments 612 the fine adjustment signal by a value equal to the operating range of the error signal, after which flow returns to step 604. The Costas phase-lock loop 100 will quickly reduce the error signal to return the adjusted error signal to its former value for maintaining lock with the radio signal. The net result will be to move the error signal to the opposite (low) limit of its operating range, thereby keeping the error signal within the predetermined operating range.

If in step 610 the error signal is not above a high limit of its predetermined operating range, then the processor 306 checks 614 whether the radio signal has been lost. If not, flow returns to step 604 to continue monitoring the error signal. If the radio signal has been lost, the processor 306 waits 616 for the signal to be reacquired and then flow returns to step 604.

As discussed above regarding step 516 (FIG. 5), it will be appreciated that either step 608 or step 612, if executed during the reception of data, would be likely to cause bit errors in the received data. Thus, the fine range control element 336 preferably also limits the execution of steps 608 and 612 to those times during which data is not being received. As stated above, such operation preferably is facilitated by designing the system such that the satellite transmissions send the data in packets of predetermined periodicity separated by intervals of no data, wherein each packet includes initial synchronization information that allows the satellite receiver

system 400 to reacquire phase lock to the radio signal following the execution of either step 608 or step 612.

Referring to FIG. 7, an electrical block diagram of an error signal monitor element in accordance with an alternative embodiment of the present invention comprises a voltage comparator 702 having a comparison output 704 coupled to the processor 306. The voltage comparator 702 compares the error signal present on the error signal output 134 of the Costas phase-lock loop 100 and the adjusted error signal present at the output of the first summing element 328. The comparison output 704 indicates to the processor 306 whether the error signal from the Costas phase-lock loop 100 is attempting to correct the adjusted error signal positively or negatively compared to the amount of correction currently provided by the fine adjustment value supplied by the control path 331. The processor 306 then readjusts the fine adjustment value towards the direction of the correction being presented by the Costas phase-lock loop 100, thereby reducing the amount of correction required therefrom. By monitoring the fine adjustment value, the processor 306 also determines when the adjusted error signal is about to go beyond its operating range on the low frequency side. Then the processor 306 controls the VCO 200 to generate a next lower predetermined frequency and simultaneously generates a new fine adjustment value to set the adjusted error signal to the opposite operating range limit on the high frequency side. In this manner the processor 306 maintains the adjusted error signal within an operating range suitable for warping the first varactor diode 212, as described herein above in regard to the preferred embodiment of the present invention.

Thus, the preferred embodiment of the present invention is a satellite receiver system that provides acquisition and frequency tracking of a Doppler shifted radio signal to allow reception of the radio signal from an orbiting satellite for substantially the entire period during which the satellite is in view of the satellite receiver system. The satellite receiver system allows a receiver bandwidth much narrower than the total range of Doppler-shifted frequencies that result from the orbital motion of the satellite relative to the receiver system. The narrow receiver bandwidth advantageously provides high receiver sensitivity, thereby allowing the transmitter power of the satellite to be substantially reduced, compared to the transmitter power that would be required for

use with a conventional receiver system having a bandwidth wide enough to lock with the total range of Doppler-shifted frequencies.

What is claimed is:

CLAIMS

1. A satellite receiver system that provides acquisition and frequency tracking of a Doppler-shifted radio signal received from an orbiting satellite, said satellite receiver system comprising:

a Costas phase-lock loop that receives the radio signal and provides an error signal at an error signal output for controlling a conversion frequency generated by a voltage controlled oscillator;

said voltage controlled oscillator coupled to said Costas phase-lock loop, wherein said voltage controlled oscillator generates the conversion frequency for down-converting the radio signal in said Costas phase-lock loop, and wherein said voltage controlled oscillator comprises a programmable frequency synthesizer that can be programmed to generate a plurality of frequencies selectable in steps; and

a Doppler frequency acquisition and tracking element coupled to said voltage controlled oscillator, wherein said Doppler frequency acquisition and tracking element adjusts the conversion frequency to compensate for a Doppler frequency shift occurring in the radio signal due to orbital motion of said orbiting satellite, and wherein said Doppler frequency acquisition and tracking element comprises:

a coarse adjustment element coupled to said programmable frequency synthesizer for selecting a suitable one of the plurality of frequencies to provide a coarse adjustment of the conversion frequency to compensate for the Doppler frequency shift; and

a fine adjustment element coupled to said error signal output for generating a fine adjustment signal at an adjusted error signal output for providing a fine adjustment of the conversion frequency to compensate for the Doppler frequency shift.

2. The satellite receiver system according to claim 1, wherein said coarse adjustment element comprises:

a power measurement element coupled to said Costas phase-lock loop for measuring received power of the radio signal; and

a coarse control element coupled to said power measurement element and coupled to said programmable frequency synthesizer, wherein, at start-up and also in response to the received power being below a predetermined threshold, said coarse control element controls said fine adjustment element to set the fine adjustment signal to a

predetermined neutral value, and thereafter controls said synthesizer to generate a predetermined sequence of frequencies from the plurality of frequencies until a frequency that results in a received power above the predetermined threshold is generated.

3. The satellite receiver system according to claim 2, wherein said fine adjustment element comprises:

an error signal monitor coupled to said error signal output for monitoring the error signal to determine whether the error signal is within a first predetermined operating range demarked by low and high limits;

a summing element coupled to said error signal output for summing the fine adjustment signal with the error signal to produce an adjusted error signal at said adjusted error signal output, wherein said adjusted error signal output is coupled to said voltage controlled oscillator for providing the fine adjustment of the conversion frequency; and

a fine range control element coupled to said summing element and coupled to said error signal monitor, wherein, after the radio signal has been acquired, said fine range control element decrements the fine adjustment signal by a fine adjustment value equal to the first predetermined operating range in response to the error signal being below the low limit, and increments the fine adjustment signal by the fine adjustment value in response to the error signal being above the high limit, thereby acting to maintain the error signal within the first predetermined operating range.

4. The satellite receiver system according to claim 3, wherein said coarse adjustment element further comprises:

an adjusted error signal monitor coupled to said error signal monitor and coupled to said fine adjustment element for monitoring the adjusted error signal to determine whether the adjusted error signal is within a second predetermined operating range demarked by first and second limits, wherein the conversion frequency corresponding to the first limit is a lower frequency than that corresponding to the second limit; and

a coarse range control element coupled to said fine adjustment element and coupled to said adjusted error signal monitor,

wherein said coarse range control element controls said synthesizer to generate a next lower one of the plurality of frequencies and simultaneously controls said fine adjustment element to set the adjusted error signal to a value substantially equal to the second limit, in response to the adjusted error signal being outside of the second predetermined operating range in a direction beyond the first limit.

5. A satellite receiver system that provides acquisition and frequency tracking of a Doppler-shifted radio signal received from an orbiting satellite, said satellite receiver system comprising:

a Costas phase-lock loop that receives the radio signal and provides an error signal at an error signal output for controlling a conversion frequency generated by a voltage controlled oscillator;

said voltage controlled oscillator coupled to said Costas phase-lock loop, wherein said voltage controlled oscillator generates the conversion frequency for down-converting the radio signal in said Costas phase-lock loop; and

Doppler frequency acquisition and tracking means coupled to said voltage controlled oscillator, wherein said Doppler frequency acquisition and tracking means adjusts the conversion frequency to compensate for a Doppler frequency shift occurring in the radio signal due to orbital motion of said orbiting satellite.

6. The satellite receiver system according to claim 5, wherein said Doppler frequency acquisition and tracking means further comprises fine adjustment means coupled to said error signal output for generating a fine adjustment signal at an adjusted error signal output for providing fine adjustment of the conversion frequency to compensate for the Doppler frequency shift.

7. The satellite receiver system according to claim 5,

wherein said voltage controlled oscillator comprises a programmable frequency synthesizer that can be programmed to generate a plurality of frequencies selectable in steps, and

wherein said Doppler frequency acquisition and tracking means comprises coarse adjustment means coupled to said programmable frequency synthesizer for selecting a suitable one of the plurality of

frequencies to provide a coarse adjustment of the conversion frequency to compensate for the Doppler frequency shift.

8. The satellite receiver system according to claim 7, wherein said Doppler frequency acquisition and tracking means further comprises fine adjustment means coupled to said error signal output for generating a fine adjustment signal at an adjusted error signal output for providing a fine adjustment of the conversion frequency to compensate for the Doppler frequency shift.

9. The satellite receiver system according to claim 8, wherein said coarse adjustment means comprises:

power measurement means coupled to said Costas phase-lock loop for measuring received power of the radio signal; and

coarse control means coupled to said power measurement means and coupled to said programmable frequency synthesizer, wherein, at start-up and also in response to the received power being below a predetermined threshold, said coarse control means controls said fine adjustment means to set the fine adjustment signal to a predetermined neutral value, and thereafter controls said synthesizer to generate a predetermined sequence of frequencies from the plurality of frequencies until a frequency that results in a received power above the predetermined threshold is generated.

10. The satellite receiver system according to claim 9, wherein said fine adjustment means comprises:

error signal monitor means coupled to said error signal output for monitoring the error signal to determine whether the error signal is within a first predetermined operating range demarked by low and high limits;

summing means coupled to said error signal output for summing the fine adjustment signal with the error signal to produce an adjusted error signal at said adjusted error signal output, wherein said adjusted error signal output is coupled to said voltage controlled oscillator for providing the fine adjustment of the conversion frequency; and

fine range control means coupled to said summing means and coupled to said error signal monitor means, wherein, after the radio signal

has been acquired, said fine range control means decrements the fine adjustment signal by a fine adjustment value equal to the first predetermined operating range in response to the error signal being below the low limit, and increments the fine adjustment signal by the fine adjustment value in response to the error signal being above the high limit, thereby acting to maintain the error signal within the first predetermined operating range.

11. The satellite receiver system according to claim 10, wherein said coarse adjustment means further comprises:

adjusted error signal monitor means coupled to said error signal monitor means and coupled to said fine adjustment means for monitoring the adjusted error signal to determine whether the adjusted error signal is within a second predetermined operating range demarked by first and second limits, wherein the conversion frequency corresponding to the first limit is a lower frequency than that corresponding to the second limit; and

coarse range control means coupled to said fine adjustment means and coupled to said adjusted error signal monitor means, wherein said coarse range control means controls said synthesizer to generate a next lower one of the plurality of frequencies and simultaneously controls said fine adjustment means to set the adjusted error signal to a value substantially equal to the second limit, in response to the adjusted error signal being outside of the second predetermined operating range in a direction beyond the first limit.

12. The satellite receiver system according to claim 11,

wherein the radio signal comprises information carried in modulation of a type selected from a group consisting of binary phase-shift keyed (BPSK) modulation, double sideband amplitude modulation, and differentially encoded BPSK modulation, and

wherein said Costas phase-lock loop comprises demodulation means for demodulating the radio signal to derive the information.

13. A satellite receiver system that provides acquisition and frequency tracking of a Doppler-shifted radio signal received from an orbiting satellite, said satellite receiver system comprising:

a Costas phase-lock loop that receives the radio signal and provides an error signal at an error signal output for controlling a conversion frequency generated by a voltage controlled oscillator;

said voltage controlled oscillator coupled to said Costas phase-lock loop, wherein said voltage controlled oscillator generates the conversion frequency for down-converting the radio signal in said Costas phase-lock loop; and

a Doppler frequency acquisition and tracking element coupled to said voltage controlled oscillator, wherein said Doppler frequency acquisition and tracking element adjusts the conversion frequency to compensate for a Doppler frequency shift occurring in the radio signal due to orbital motion of said orbiting satellite.

14. The satellite receiver system according to claim 13, wherein said Doppler frequency acquisition and tracking element further comprises a fine adjustment element coupled to said error signal output for generating a fine adjustment signal at an adjusted error signal output for providing fine adjustment of the conversion frequency to compensate for the Doppler frequency shift.

15. The satellite receiver system according to claim 13,

wherein said voltage controlled oscillator comprises a programmable frequency synthesizer that can be programmed to generate a plurality of frequencies selectable in steps, and

wherein said Doppler frequency acquisition and tracking element comprises a coarse adjustment element coupled to said programmable frequency synthesizer for selecting a suitable one of the plurality of frequencies to provide a coarse adjustment of the conversion frequency to compensate for the Doppler frequency shift.

16. The satellite receiver system according to claim 15, wherein said Doppler frequency acquisition and tracking element further comprises a fine adjustment element coupled to said error signal output for generating a fine adjustment signal at an adjusted error signal output for providing a fine adjustment of the conversion frequency to compensate for the Doppler frequency shift.

17. The satellite receiver system according to claim 16, wherein said coarse adjustment element comprises:

a power measurement element coupled to said Costas phase-lock loop for measuring received power of the radio signal; and

a coarse control element coupled to said power measurement element and coupled to said programmable frequency synthesizer, wherein, at start-up and also in response to the received power being below a predetermined threshold, said coarse control element controls said fine adjustment element to set the fine adjustment signal to a predetermined neutral value, and thereafter controls said synthesizer to generate a predetermined sequence of frequencies from the plurality of frequencies until a frequency that results in a received power above the predetermined threshold is generated.

18. The satellite receiver system according to claim 17, wherein said fine adjustment element comprises:

an error signal monitor coupled to said error signal output for monitoring the error signal to determine whether the error signal is within a first predetermined operating range demarked by low and high limits;

a summing element coupled to said error signal output for summing the fine adjustment signal with the error signal to produce an adjusted error signal at said adjusted error signal output, wherein said adjusted error signal output is coupled to said voltage controlled oscillator for providing the fine adjustment of the conversion frequency; and

a fine range control element coupled to said summing element and coupled to said error signal monitor, wherein, after the radio signal has been acquired, said fine range control element decrements the fine adjustment signal by a fine adjustment value equal to the first predetermined operating range in response to the error signal being below the low limit, and increments the fine adjustment signal by the fine adjustment value in response to the error signal being above the high limit, thereby acting to maintain the error signal within the first predetermined operating range.

19. The satellite receiver system according to claim 18, wherein said coarse adjustment element further comprises:

an adjusted error signal monitor coupled to said error signal monitor and coupled to said fine adjustment element for monitoring the

adjusted error signal to determine whether the adjusted error signal is within a second predetermined operating range demarked by first and second limits, wherein the conversion frequency corresponding to the first limit is a lower frequency than that corresponding to the second limit; and

a coarse range control element coupled to said fine adjustment element and coupled to said adjusted error signal monitor, wherein said coarse range control element controls said synthesizer to generate a next lower one of the plurality of frequencies and simultaneously controls said fine adjustment element to set the adjusted error signal to a value substantially equal to the second limit, in response to the adjusted error signal being outside of the second predetermined operating range in a direction beyond the first limit.

20. The satellite receiver system according to claim 19,

wherein the radio signal comprises information carried in modulation of a type selected from a group consisting of binary phase-shift keyed (BPSK) modulation, double sideband amplitude modulation, and differentially encoded BPSK modulation, and

wherein said Costas phase-lock loop comprises a demodulation element for demodulating the radio signal to derive the information.

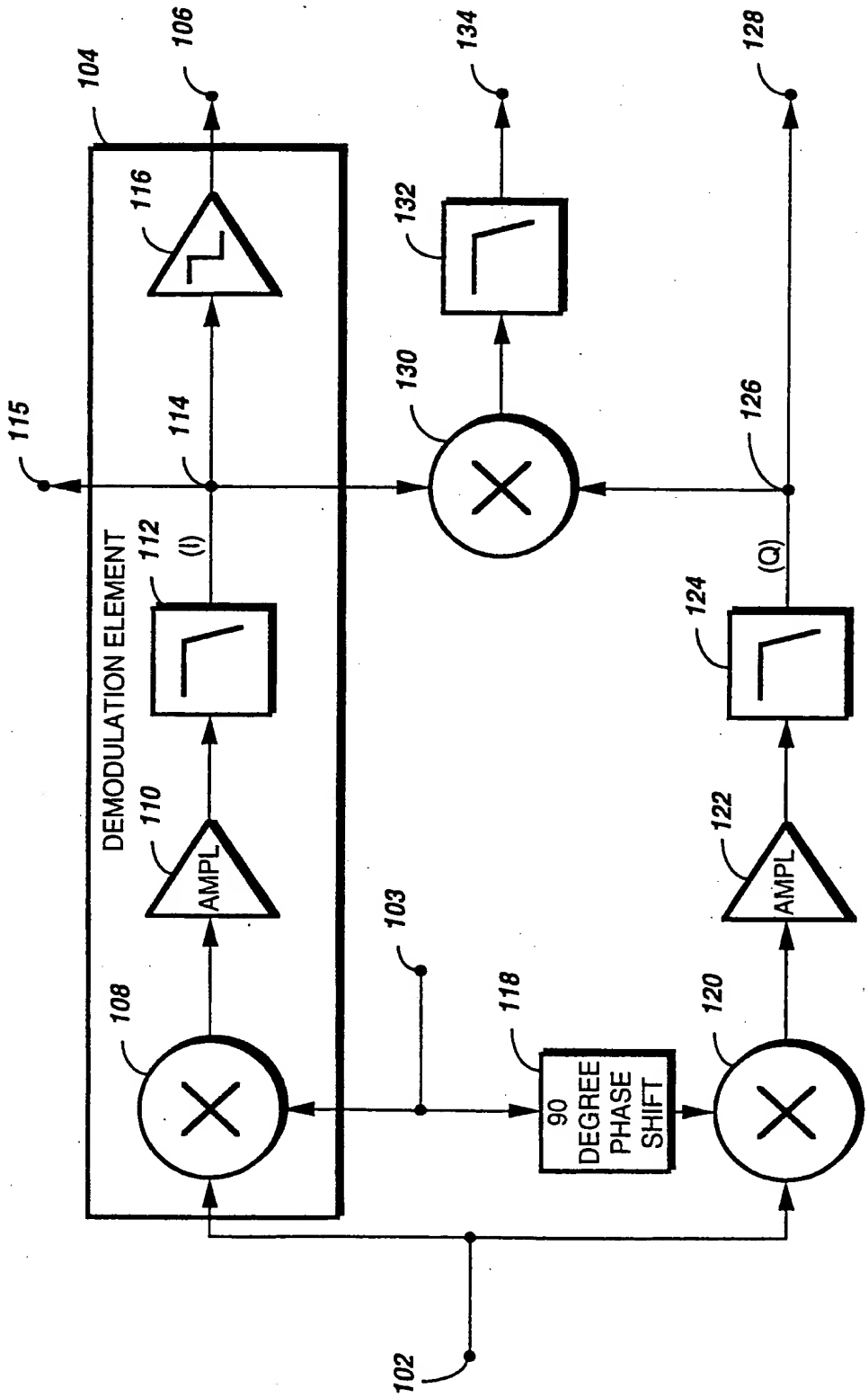
DEMODULATION ELEMENT
AMPL
AMPL
90 DEGREE PHASE SHIFT
(I)
(Q)
100
PRIOR ART

FIG. 1

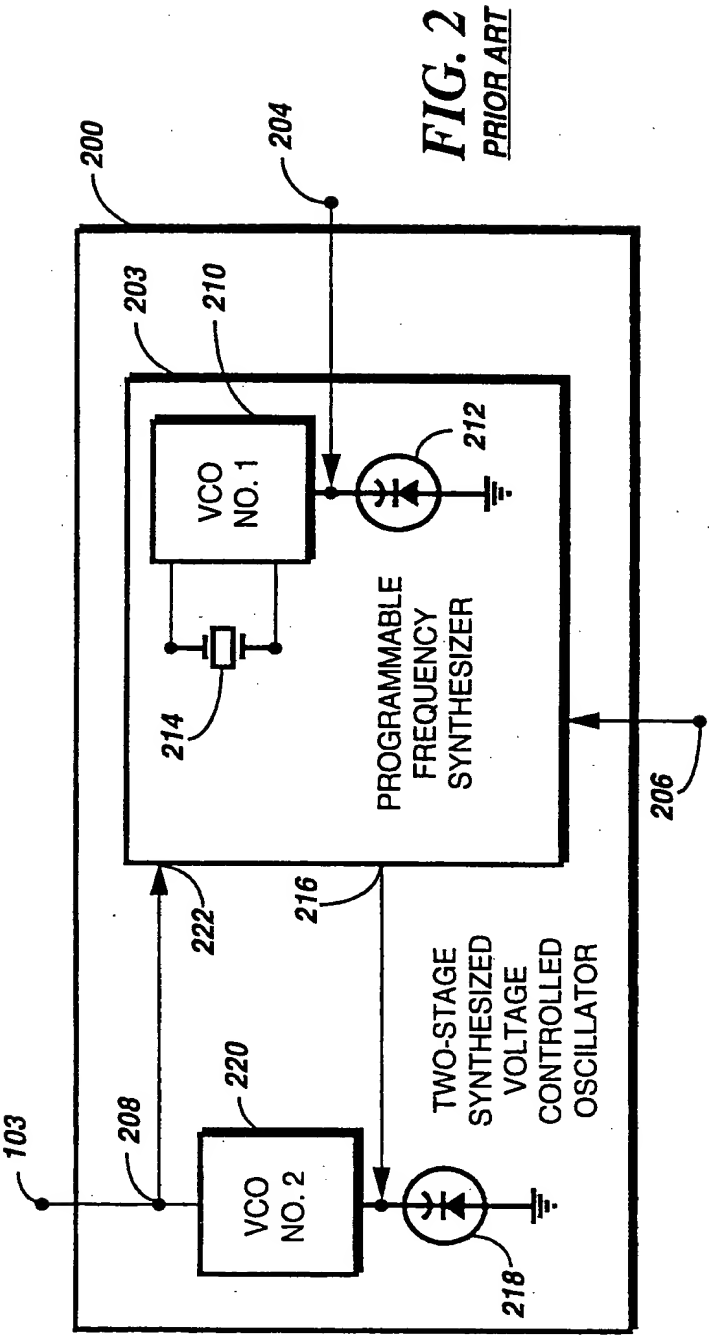

FIG. 2
PRIOR ART

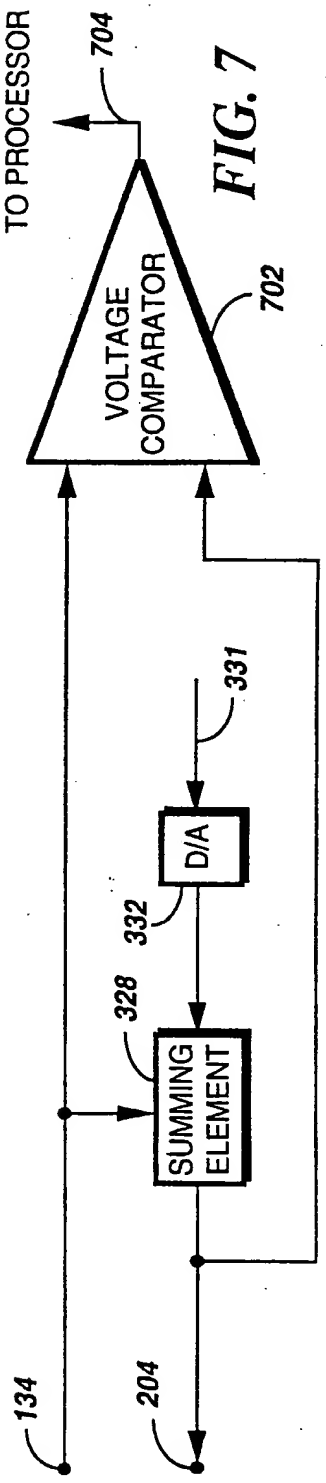

FIG. 7

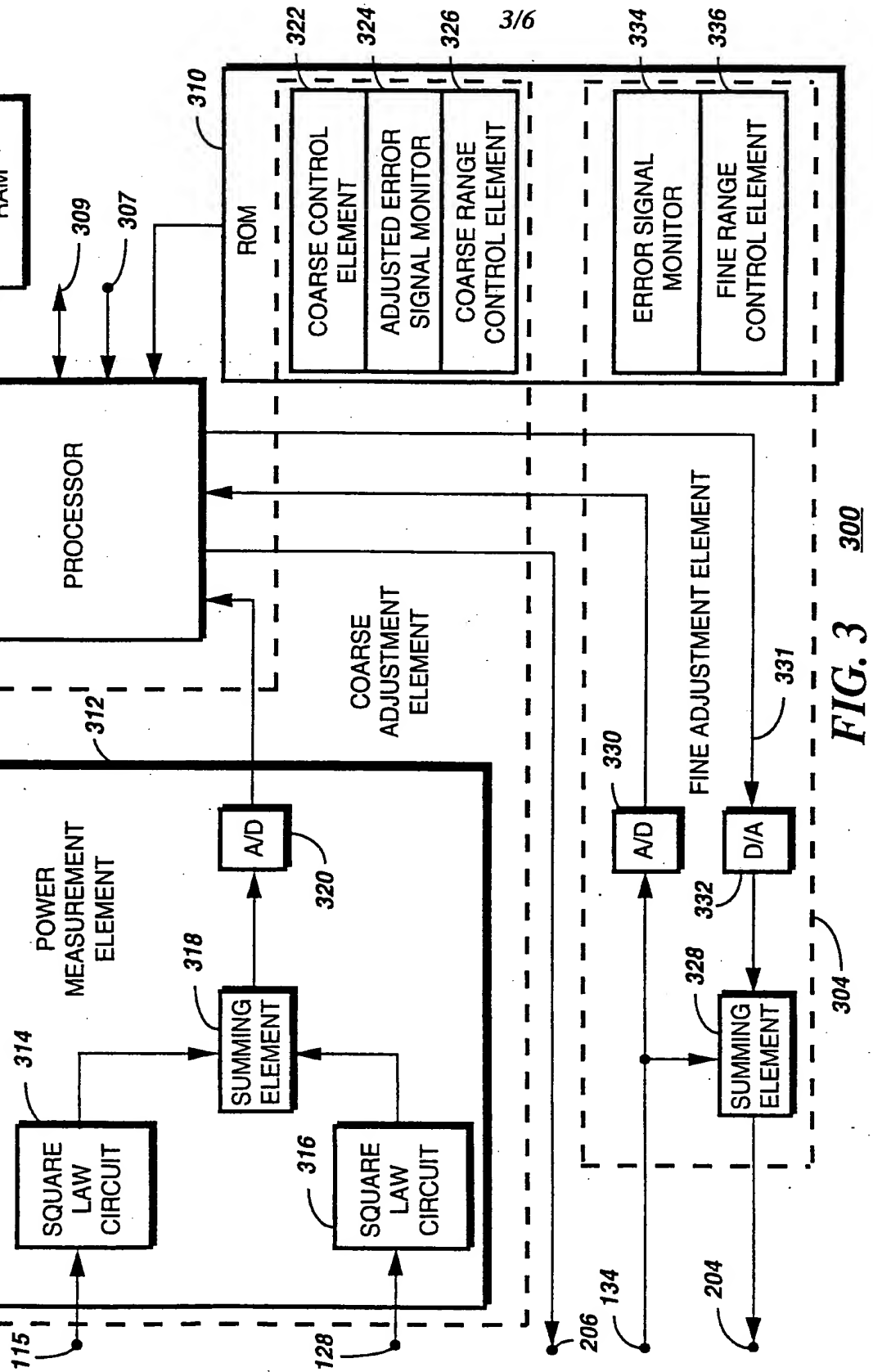
3/6
322
324
326
334
336
310
308
RAM
309
307
ROM
COARSE CONTROL ELEMENT
ADJUSTED ERROR SIGNAL MONITOR
COARSE RANGE CONTROL ELEMENT
ERROR SIGNAL MONITOR
FINE RANGE CONTROL ELEMENT
306
PROCESSOR
302
312
COARSE ADJUSTMENT ELEMENT
FINE ADJUSTMENT ELEMENT
331
330
POWER MEASUREMENT ELEMENT
A/D
320
A/D
D/A
332
318
328
304
SUMMING ELEMENT
SUMMING ELEMENT
314
SQUARE LAW CIRCUIT
316
SQUARE LAW CIRCUIT
115
128
206
134
204

FIG. 3 300

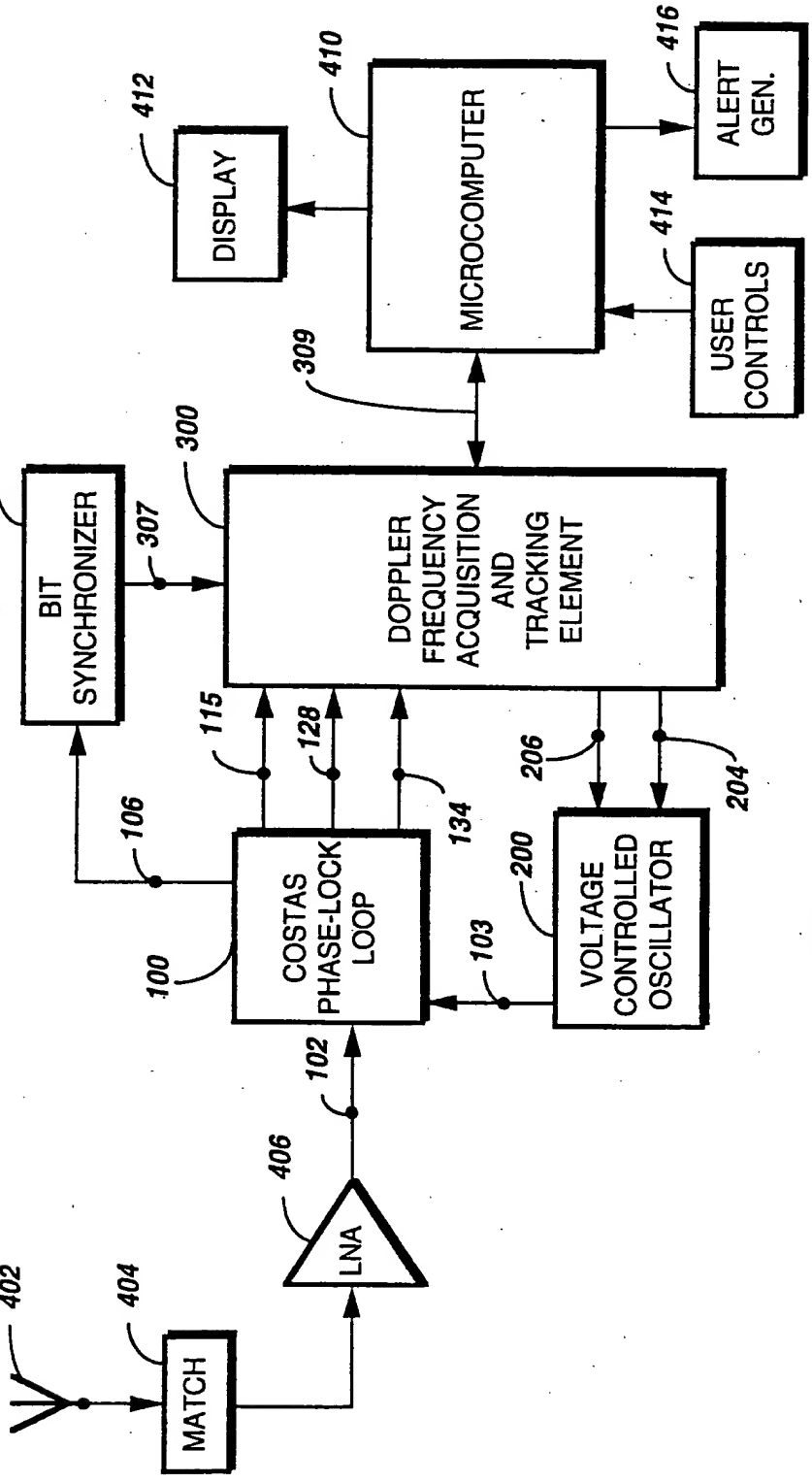
402
404
MATCH
406
LNA
102
100
COSTAS PHASE-LOCK LOOP
103
200
VOLTAGE CONTROLLED OSCILLATOR
106
115
128
134
206
204
408
BIT SYNCHRONIZER
307
300
DOPPLER FREQUENCY ACQUISITION AND TRACKING ELEMENT
309
412
DISPLAY
410
MICROCOMPUTER
414
USER CONTROLS
416
ALERT GEN.

FIG. 4

400

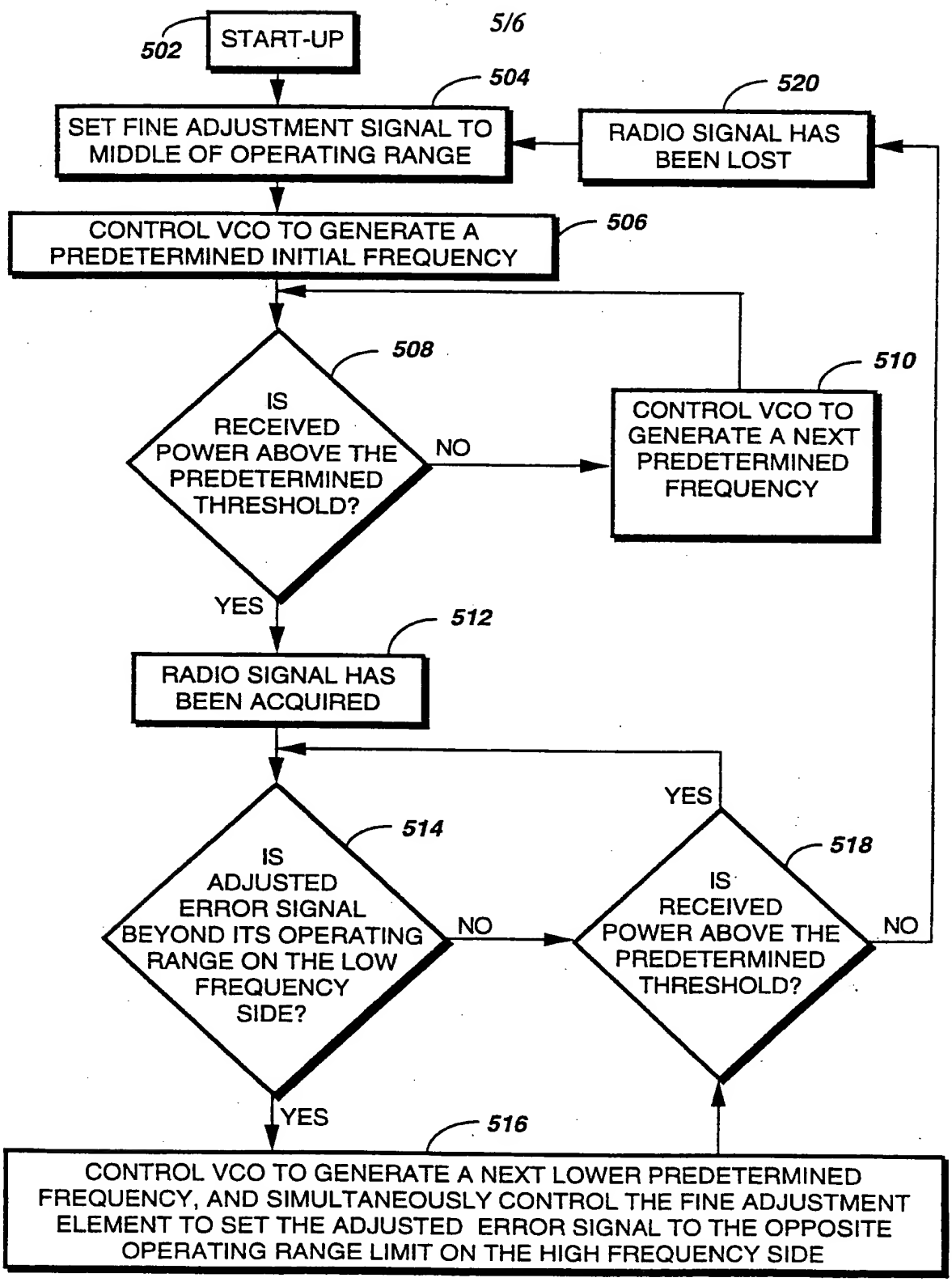
502
START-UP
504
SET FINE ADJUSTMENT SIGNAL TO MIDDLE OF OPERATING RANGE
520
RADIO SIGNAL HAS BEEN LOST
506
CONTROL VCO TO GENERATE A PREDETERMINED INITIAL FREQUENCY
508
IS RECEIVED POWER ABOVE THE PREDETERMINED THRESHOLD?
NO
510
CONTROL VCO TO GENERATE A NEXT PREDETERMINED FREQUENCY
YES
512
RADIO SIGNAL HAS BEEN ACQUIRED
514
IS ADJUSTED ERROR SIGNAL BEYOND ITS OPERATING RANGE ON THE LOW FREQUENCY SIDE?
NO
YES
518
IS RECEIVED POWER ABOVE THE PREDETERMINED THRESHOLD?
NO
YES
516
CONTROL VCO TO GENERATE A NEXT LOWER PREDETERMINED FREQUENCY, AND SIMULTANEOUSLY CONTROL THE FINE ADJUSTMENT ELEMENT TO SET THE ADJUSTED ERROR SIGNAL TO THE OPPOSITE OPERATING RANGE LIMIT ON THE HIGH FREQUENCY SIDE

FIG. 5

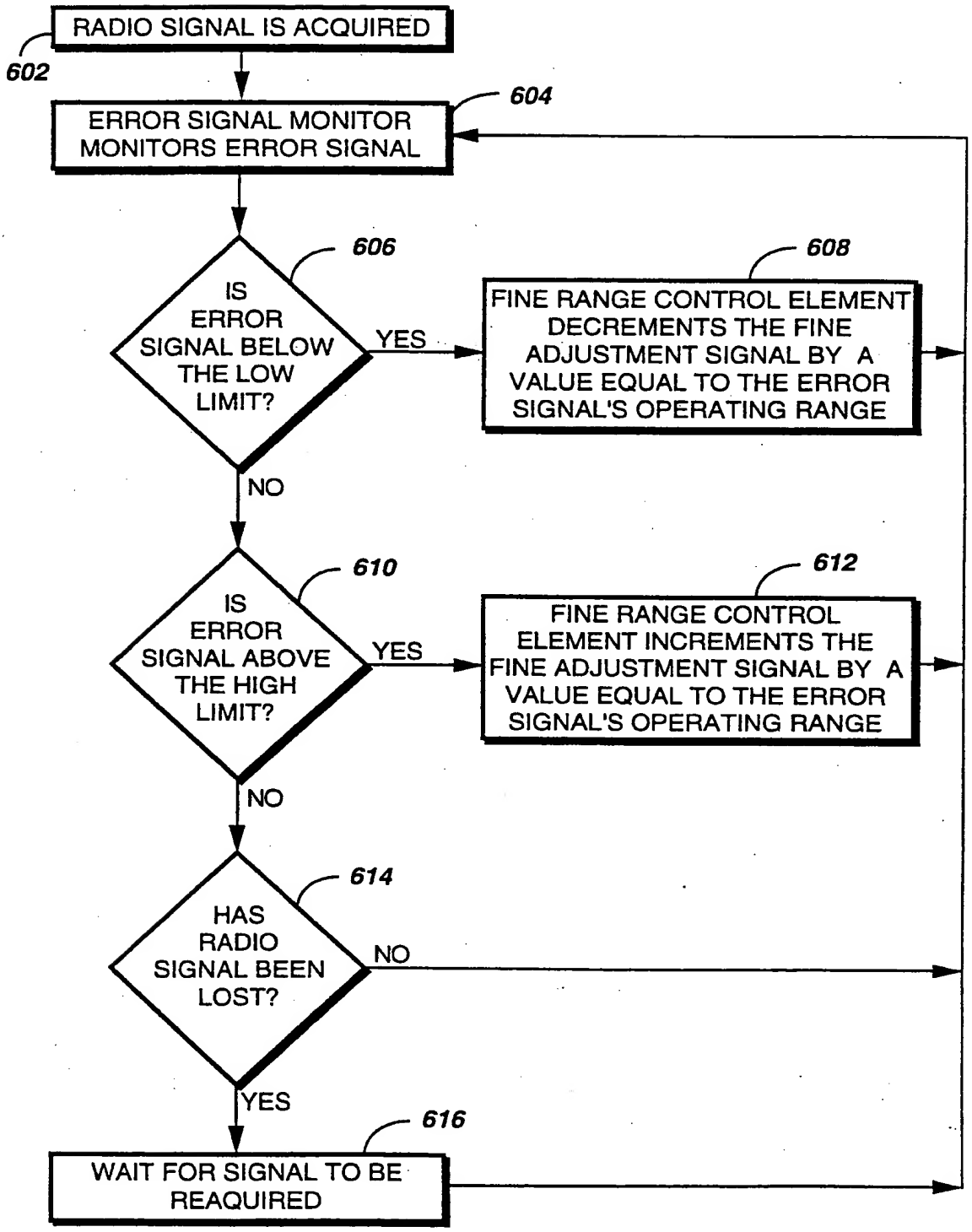
RADIO SIGNAL IS ACQUIRED
602
ERROR SIGNAL MONITOR MONITORS ERROR SIGNAL
604
IS ERROR SIGNAL BELOW THE LOW LIMIT?
606
YES
FINE RANGE CONTROL ELEMENT DECREMENTS THE FINE ADJUSTMENT SIGNAL BY A VALUE EQUAL TO THE ERROR SIGNAL'S OPERATING RANGE
608
NO
IS ERROR SIGNAL ABOVE THE HIGH LIMIT?
610
YES
FINE RANGE CONTROL ELEMENT INCREMENTS THE FINE ADJUSTMENT SIGNAL BY A VALUE EQUAL TO THE ERROR SIGNAL'S OPERATING RANGE
612
NO
HAS RADIO SIGNAL BEEN LOST?
614
NO
YES
WAIT FOR SIGNAL TO BE REAQUIRED
616

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/00325

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H04B 7/185; G01S 5/02
US CL :342/357
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 342/357

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 4,088,955 (BAGHDADY) 09 May 1978, see entire document.	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 18 APRIL 1995	Date of mailing of the international search report 16 MAY 1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer THEODORE BLUM Telephone No. (703) 308-0481

Form PCT/ISA/210 (second sheet)(July 1992)*